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APB Process Timing

Introduction

The following application note addresses timing specific issues and techniques which may be helpful when designing systems with the APB and SR micro-PLC products. The focus is directed towards the APB family of controllers, with notes indicating major differences for the SR family.

Programming Support

The APB product is programmed using a Functional Block programming language. Each operation to be performed is represented by a function block and the function blocks are configured using the design software - SuperCad for SR controllers and APBSoftware for APB controllers.

NOTE: Although very similar in operation these products are not directly compatible and programs may not be directly transferred from one product to another.

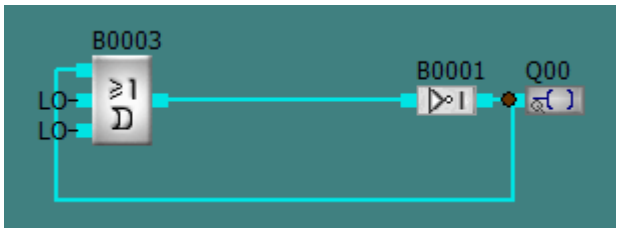
Execution Speed.

In a vast majority of applications the APB or SR controller will process the overall program much faster than required by the physical system. In critical programming situations it may be necessary to review exactly how fast the micro-PLC will respond to a particular set of inputs and how quickly the controller can change the outputs.

Programs consist of a number of 'function' blocks – up to 320 for the APB controller and 128 for the SR controller. When a program is executing it processes the function blocks in a 'round robin' sequence. It will process block B0000, then block B0001, then B0002 etc. until all the blocks have been processed. The controller will then update the physical I/O and restart the processing at block B0000.

The overall time required to perform all the processing determines how quickly the controller will respond to a change in an input and how quickly an output can change. For example, if very short 'pulses' of 100 usec are applied to an input and the program only samples the input every 50 msec the signal will be either missed or only randomly detected leading to very erratic behavior.

The absolute 'minimum' program on an APB controller, shown below, generates a square wave output at 250 hertz. When connected to an oscilloscope the output is ON for 2 msec and then OFF for 2 msec, indicating that each program sequence requires 2 msec.



In this circuit, the blocks B0001 and B0003 form a 'free running' oscillator. If the output Q00 is ON during a particular program scan the state will be inverted by B0001 and turned OFF on the next program scan. The OR block B0003 is required since a block's input can not be directly connect to its own output. The OR gate can be replaced with a PONS timer in which case the pulse rate generated will be determined by the Pulse Time of the PONS block. The PONS Reset signal may be used to enable/disable the oscillator.

NOTE: This circuit works for solid state outputs. It is not recommended on RELAY based outputs.

Having established the maximum sampling rate of an APB controller it is then possible to determine the time required to process an actual program that will contain a variable number of function blocks of a variable complexity.

The time taken to process a specific function block is determined by the complexity of the block function and whatever auxiliary actions must be performed based on the function blocks' current values. For example, simply incrementing a value (counter) requires very little processing time as compared to performing a division on an numeric value. If the counter has a comparator which has be be verified and possibly an output to be activated this will add a variable execution time.

Since the intent is to determine the worst case timing a MATH block with 3 divisions was chosen: result = V1 / V2 / V3 / V4. To simplify the measurement, 10 such blocks were loaded, each performing the same 3 division operations.

Using the same free running oscillator with the added 10 MATH blocks resulted in a square wave of 200 Hertz, implying that the 10 MATH blocks each added ~ 50 usec of processing time.

Repeating the same test but using 10 UDCT (counters) affected the overall cycle time by ~ 10 usec per counter. It is reasonable to assume that in a real-world situation the processing of each function block will range from less than 10 usec to ~ 50 usec.

To arrive at a 'worst case' situation for an APB controller, and assuming all 320 function blocks required 50 usec to process (VERY UNLIKELY) it implies that an allowance must be made for an additional 16 msec for each program scan, resulting in an overall worst case of ~ 18 msec/program scan. A much more 'likely' performance number would be 10 usec X 320 + 2 msec ~ 5 msec.

These numbers will be further impacted if additional I/O Expansion modules have been added or an external Modbus interface is in use. The measured times do provide an 'order of magnitude' as far as the expectation of processing speed.

High Speed I/O

DC powered APB controllers have several function blocks that support motion control and higher speed I/O operations: four dedicated inputs (I4..I7) and 2 dedicated outputs (DC powered solid state outputs only) that support signals up to 10 kHz.

The SR family does not support high speed I/O.

Function blocks related to counting activities (counters, frequency monitors) accept High Speed inputs (I04..I07) to the CNT (TRG) input signal.

The high speed inputs only affect the CNT signal on the UDCT and UDCF. The DIR signal is processed using standard I/O and is limited to 40 msec sampling as described above. This limits the counter speed where quadrature inputs are used.

The Two Phase Counter (2PCT) allows both signal A and signal B to be connected to high speed inputs aw well as support 1, 2, or 4 times count sequencing specifically for quadrature input processing.

Function	Description
UDCT	Up/Down Counter, Count and Direction.
UDCF	Up/Down Counter, Count and Direction with Low/High comparator

FTH	Frequency Threshold Trigger. Verifies signal within a specified frequency range
A+B-	Up/Down Counter with Count Up and Count Down inputs
2PCT	Two Phase Counter. 1, 2 or 4 X multiplier, quadrature inputs

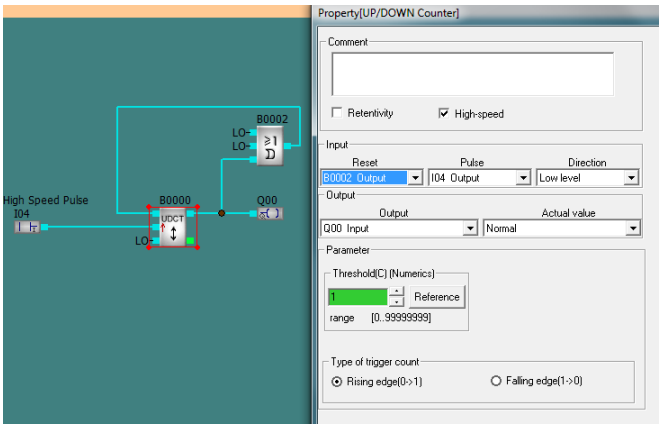
The following table lists the function blocks that generate high speed outputs (Q02, Q03).

Function	Description
PTO	Generates pulse train of 'N' pulses at a variable frequency.
PWM	Generates a pulse train of 'N' pulses with a variable duty cycle and frequency.
ACC	Generates a pulse train of 'N' pulses at a 50 % duty cycle. The frequency is ramped up, held constant and then ramped down.

Capturing High Speed Pulses

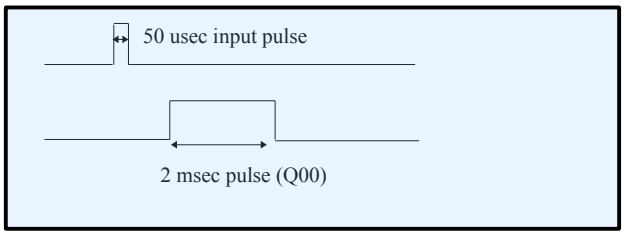
As noted above, high speed pulses can not be reliably captured by standard function blocks. If high speed pulses must be captured and processed they may be connected to an UDCT with the preset set to 1 and reset connected (thru an intermediate function block) to the UDCT output.

In operation, the high speed pulse will increment the counter independent of the block process sequence. On the next program scan the counter will be compared to the preset value (1) and the counter output will be set active (ON). The active output can be processed using standard function blocks and the counter will be reset. Note an OR block is used to satisfy the APBSoftware requirement that a block input cannot be connected directly to it's output.



The other requirement is that the 'high speed' option is selected in the UDCT parameter setup screen. This option will only be effective if the input selected is one of I04..I07.

Figure 1 – High Speed Pulse Capture



Block Processing Sequence.

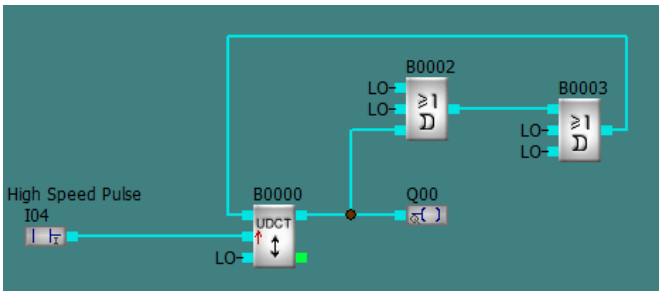
As previously mentioned, the application program within an APB or SR micro-PLC consists of a number of function blocks which are sequentially processed. At the end of the process scan the physical I/O is updated and the cycle repeats.

Each function block is automatically assigned a block number by the development software when it is placed on the circuit. The development software

allows the user to manually change the block numbers for special situations.

In the majority of situations the exact order of processing is not significant and the programmer can rely on the APBSoftware (or SuperCAD) to automatically assign the block numbers.

In specific situations the processing sequence is important. The previous example has been modified by adding a second OR block in the reset feedback loop.

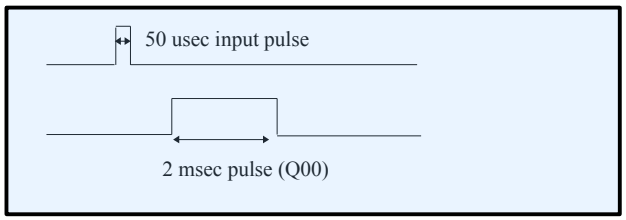


In the example shown above, block B0002 is connected to the UDCT block and the output of B0002 is connected to the 2nd OR block B0003 which drives the UDCT reset pin.

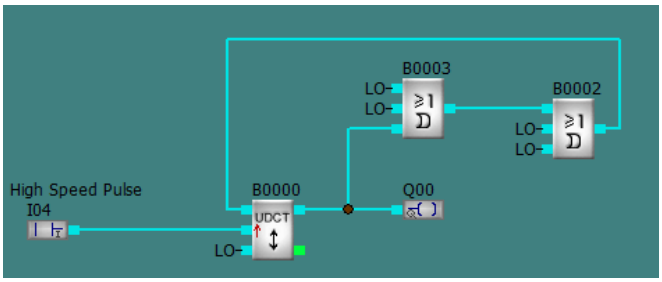
During the sequential processing, when the UDCT output becomes active (ON) it is processed by B0002, which sets it's output active (ON). The 2nd OR block B0003 is then processed and since it's input is ON it will set it's output ON. During the following process scan the ON state of B0003 is applied to the UDCT reset.

The output as measured at Q01 is the same as in the circuit that contained a single OR block in the feedback loop.

Figure 2 – Dual OR block Feedback

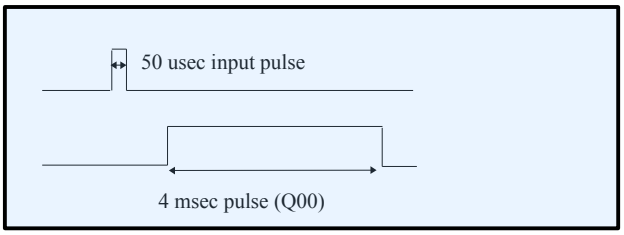


By re-ordering the function blocks as shown below we change the operation of the circuit.



In the circuit shown, the pulse is counted asynchronously using the high speed input. On the next program scan the UDCT block B0000 output is set to 1. Block B0002 is then processed but since B0003 has not yet been processed its output is still OFF and B0002 sets its output OFF. Block B0003 is then processed and since the output of the UDCT is ON it will set its output ON. On the 2nd program scan block B0002 will see's its input as ON and will set its output ON. On the third process scan the ON state of B0002 will reset the UDCT counter. The output as measured on Q00 shows that the UDTC output stays ON for two program scan times.

Figure 3 – Affects of Block Sequences



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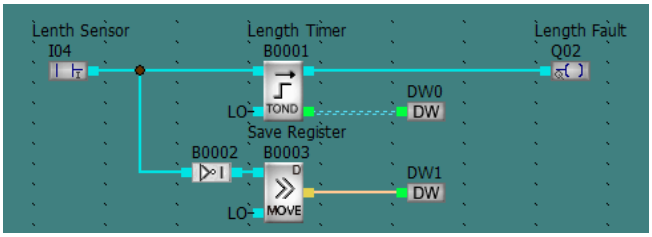
The sequential processing of blocks may be used to cause a specific sequence of events. In the following circuit a signal of duration 'N' msec is to be measured. At the trailing edge of the signal we need to latch the measured time and reset the timer.



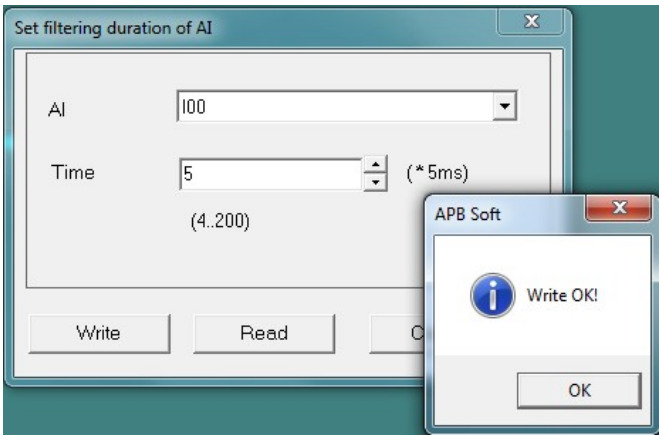
The signal is applied to a TOND timer block which will start timing when the Length Sensor signal transitions from 0 to 1. The Length Sensor signal is inverted by block B0002 and when the signal transitions from 1 to 0 the inverter will cause a 0 to 1 transition to the MOVE block B0003 trigger which will transfer the current value of the TOND (DW0) to the holding register DW1 for further processing. When the Length Signal again transitions from 0 to 1 at the next item to be measured the Length Timer will be reset and restart the timing operation. The previously measured length will remain available in DW1 for processing until the second length measurement is complete.

Digital Filtering

The inputs on APB controllers are digitally filtered to remove unwanted noise on the signals. Mechanical switches and relays in particular are known to generate 'contact bounce', where the contacts physically bounce open and closed both during closure and opening. This contact noise is very brief and can be easily filtered out.

Another source of noise is radiated electrical noise caused by inductive loads (relays, starters) and motors. This is typically at some harmonic of 60 (or 50) hertz and although more problematic in analog signals can still cause troubles with digital signals.

The APB controllers provide a default digital filter time of 50 msec, which may be adjusted between 20 msec to 1 second in 5 msec steps for each input using the APBSoftware. The Options → Set Filter Parameter screen is shown below.



NOTE: The filter parameters are not loaded as part of the application program. The APBSoftware directly sets the filter parameter within the APB controller, which is saved in non-volatile memory so that is is available after power cycles. If a new device is being installed the filter parameters must be set in addition to loading the application program.

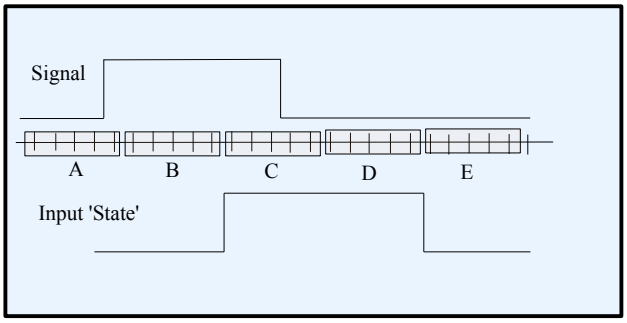
The digital filtering is not applied to the high speed digital inputs.

To understand how the filtering operates and affects digital inputs it must be noted that on the APB DC powered controllers the input circuits operate as either analog or digital inputs. If the signal level is below ~ 5 Vdc it is treated as a logical

'0', or OFF and if greater than ~ 8.5 Vdc it is treated as a logical '1', or ON .For analog signals the input voltage level is averaged over the sample period.

The digital filtering samples the signal level over the specified period and if the signal changes it leaves the calculated input 'state' unchanged. If the signal level stays at a constant level over the sampling period the input state is set corresponding to the stable level. This introduces a 'delay' in reporting a change in the input level of between 1 and 2 times the filtering time and possible pulse 'stretching' of up to 1 filter time.

Figure 4 – Digital Sampling



In Figure 4 there are 5 sample periods labeled A..E, each consisting of 5 'sample' points. During sample period A the input level changes and so at the end of the sample period the input 'State' is left unchanged at 0. During sample period B the input is at a constant high level and at the end of the sample period the input 'State' will be set to 1. During sample period C the input level changes (high to low) and so the input 'State' is not changed. During sample period D the input level is at a constant low and at the end of the sample period the input 'State' is set to 0. During sample period E the level is at a constant low and the input 'State' is set to 0.

Depending on the phase relationship between the sampling periods and the input level the input 'State' transitions from either the 'ON' state or the 'OFF' state can vary by up to 1 sample period.

NOTE: It is generally a safe practice to set the sampling rate to be at least twice of the highest expected signal frequency. For example, if input signals of 10 Hertz (100 msec) are expected the sampling period should be no more than 50 msec.

The APB controller allows a minimum sampling period of 4 X 5 = 20 msec, indicating that the absolute maximum input signal frequency is 50 Hertz. Observing the 2 X rule, this limits the signal to 25 Hertz.

Anti-Aliasing

Whenever an analog signal is digitally sampled harmonic components are introduced due to aliasing. Extensive literature is available on aliasing and its effects (see references).

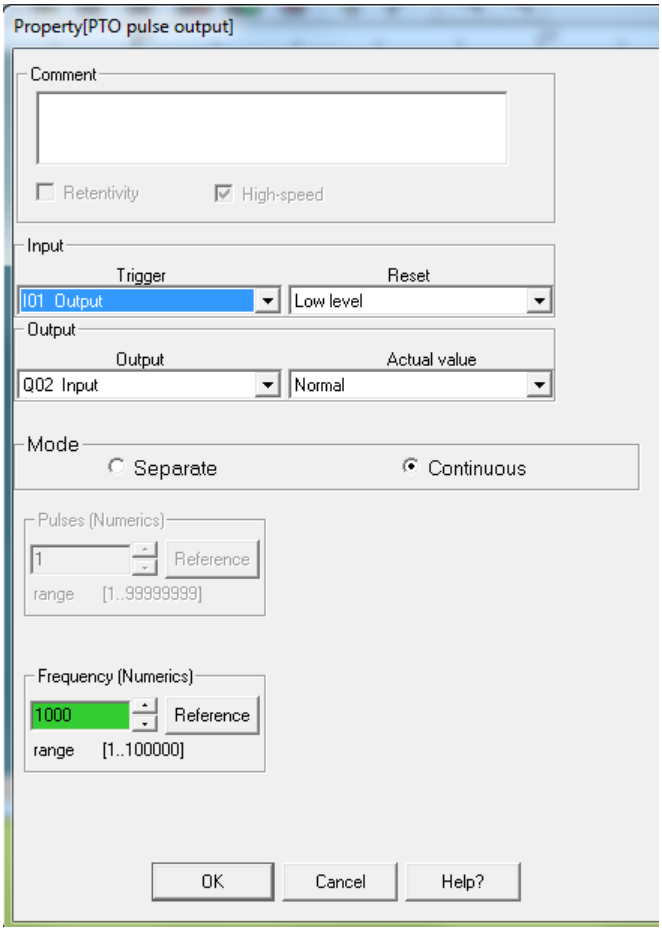
To avoid aliasing effects the Nyquist criteria should be observed which states that the sampling frequency should be limited to 2 X the maximum useful signal frequency. For inputs that are used to process varying analog signals the input filtering should be set to 2 X the maximum expected frequency.

High Speed Outputs

DC powered controllers are available with both relay and solid state (Sink or Source) outputs. Outputs which are driven by the standard function blocks will be limited to the program scan times as described above. Clearly, relay output rates will be limited to the mechanical action of the relays.

As noted, there are three function blocks that provide high speed outputs and there are two dedicated outputs on DC powered devices with solid state outputs (Q02, Q03) available for these functions.

The PTO function block will generate a stream of pulses with a 50 % duty cycle. The number of pulses and the frequency of the pulse stream may be specified using constant values or values derived from internal Data Registers DW0..DW255.



The PTO will generate the specified number of pulses or may be configured to run continuously. Note that the Trigger input must transition from 0 to 1 to initiate the pulse generation and that the output must be Q02 or Q03. The High Speed option is always enabled. The PWM is similar to the PTO but the output pulse duty cycle, which may be a constant or derived from a Data Register may be varied from 10 to 100 %.

Motor Control

Motors must often be accelerated and decelerated to effect smooth control. In the case of stepper motors it is imperative that the step rate is ramped to avoid the motor from stalling.

The ACC function block ramps the output frequency from a low frequency to a high frequency, runs at the constant (high) frequency and then ramps the output back down to the low frequency. The low and high frequency, the total number of pulses and the number of steps used during the acceleration and deceleration phases may be all specified as constants or Data Register values.

Similar to the PTO and PWM the trigger input must transition from 0 to 1 to initiate the frequency generation and must remain at 1. If the enable signal is removed prior to the specified number of pulses the block immediately enters the deceleration phase.

Variable Duty Cycle PWM

The ACC function provides a smooth ramp of a frequency between the 'low' frequency and 'high' frequency. In DC motor drives and other applications it is common to use a PWM output and ramp the duty cycle from a 'low' value to 'high' value, thereby providing a smooth increase in the power applied to the device.

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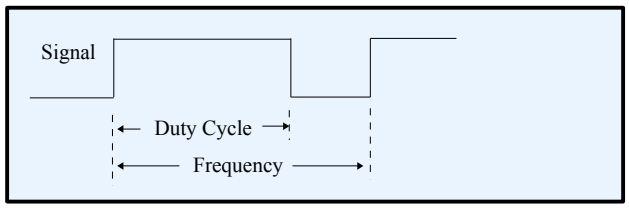
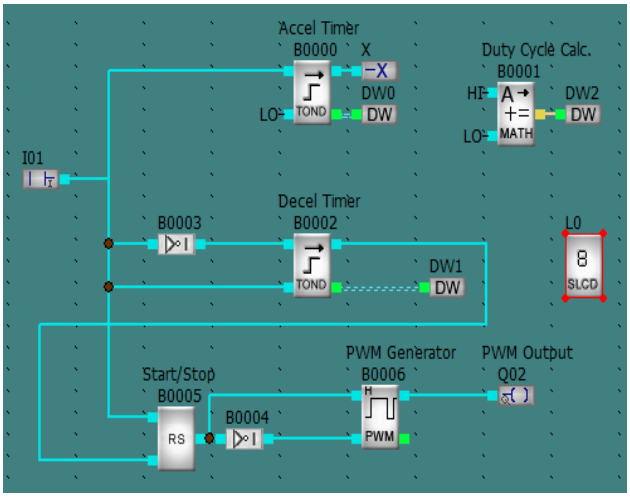
The PWM function block provided on the APB controller allows the duty cycle (the percentage of time the pulse is ON over the overall pulse period) to be set to a constant or driven by a Data Register value.

Figure 5 Duty Cycle vs. Frequency



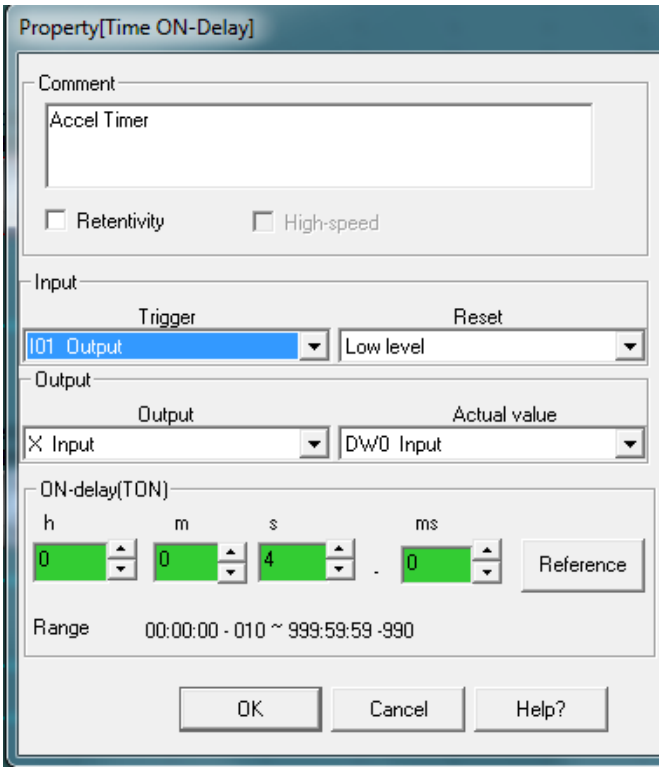
For a particular application assume that when a contact is closed an actuator must have power ramped from 10 to 90% over a 4 second period. The power should be then maintained at 90% until the contact is broken and then the power must be ramped down from 90% to 10% and then turned off. Furthermore, if the contact is broken before power has reached 90% (4 seconds) the ramp down should begin immediately back to 10% prior to shutting off the power. The power is controlled using a PWM signal operating at a fixed 100 hertz frequency.

Several of the previously discussed techniques may be used to arrive at the solution, shown below.



Block B0000, a Timer On Delay (TOND) function is used for the acceleration timer. When the signal is applied (0 to 1 transition) the timer is reset and begins timing. The Time ON value is set to 4 seconds, representing the desired acceleration time.

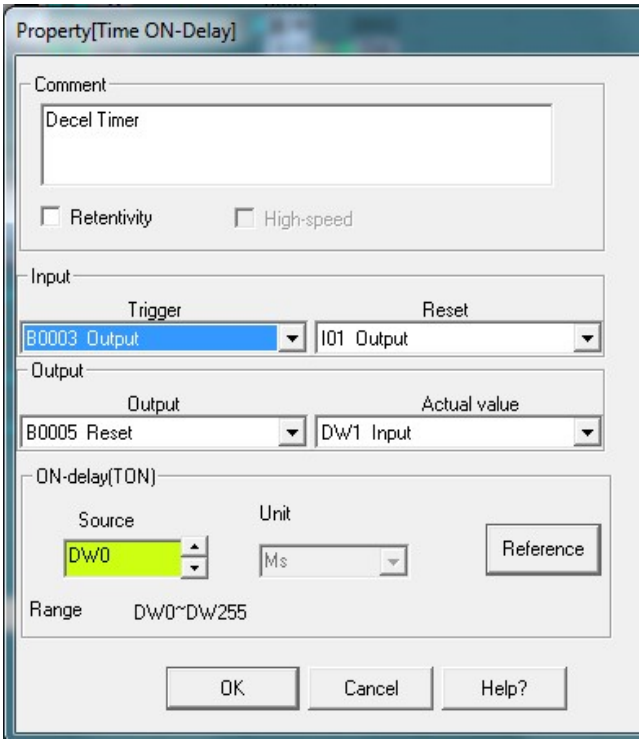
The digital output is not used and is connected to an 'unused output X' to avoid error messages from the APBSoftware regarding unconnected outputs. The actual timer value, which will ramp from 0 to 4.000 seconds, is connected to Data Register DW0.



Block B0002, another TOND function is used for the deceleration timer. The input signal is inverted by B0003 and applied to the Trigger input, providing a 0 to 1 transition when the activation signal is removed that is used to start the deceleration timer. To handle the case in which the signal is removed before the 4 second acceleration has been

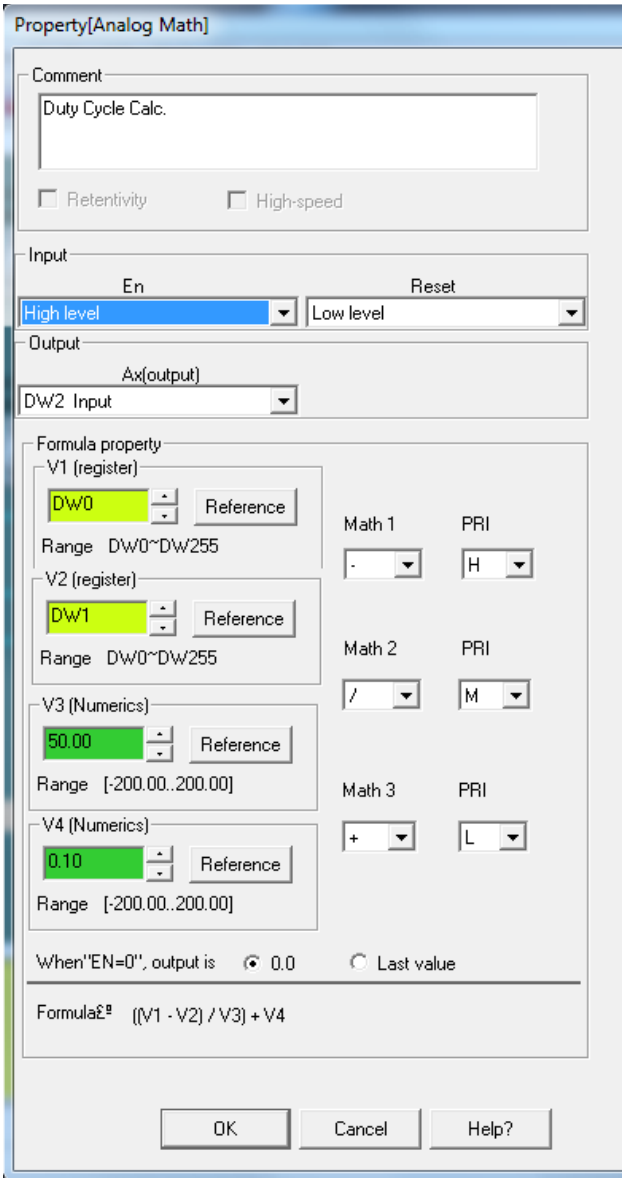
completed the TON value is linked to Data Register DW0 which contains the previous acceleration time.

When the deceleration timer reaches the TON value it will set its output active, used in the Start/Stop circuit. The actual timer value is transferred to Data Register DW1.



The third part of the circuit is implemented using a MATH function, block B0001 where the duty factor is calculated using the current values of DW0 and DW1.

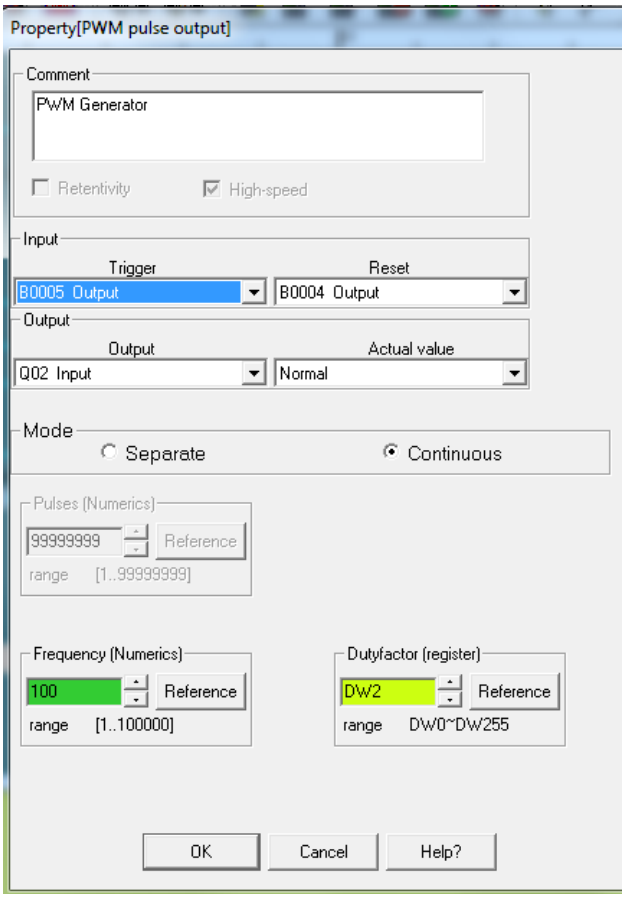
During the acceleration phase DW0 will be incrementing from 0 to 4.000 seconds and DW1 will be 0. When the 4 seconds have elapsed DW0 will be held a constant 4.000 seconds. When the signal is removed to start the deceleration DW0 will be maintained and DW1 will start incrementing from 0 to the TON value, the time elapsed during the acceleration phase. By subtracting the DW1 value from DW0 will result in a number that ramps from 0 to 4.000 and then ramps down from 4.000 to 0. This value is divided by 50 to provide a number from 0 to .80 and finally a constant of .10 is added to result in a number ranging from .10 to .90.



The output from the MATH block is connected to Data Register DW2.

NOTE: The MATH function block operates on fixed point arithmetic values, where there is an implied decimal point between the 2nd and 3rd digit. Internally, the integer value 123 will be displayed as 1.23. In our case, the fractional value of .10 is internally an integer value of 10 and the .90 is an integer value of 90.

The last portion of the circuit consists of the PWM pulse generator B0006 and the Start/Stop reset circuit consisting of an RS latch B0005 and an inverter B0004.



The PWM frequency is fixed at 100 hertz and the 'continuous' mode is selected so that pulses will be generated as long as the Trigger is held active. The Duty Factor is connected to the DW2 value, calculated by the MATH function block.

The Start/Stop reset circuit controls the sequencing of the overall circuit and is sensitive to the processing sequence of the blocks. When the Activation signal transitions from 0 to 1 the Deceleration timer (B0002) is reset which in turn removes the Reset Signal from the Start/Stop latch. The Activation signal, applied to the Set input, causes the Reset Latch B0005 to switch to ON state. Since the Reset Latch block number is numerically higher than the Inverter B0004 it will not be applied to the PWM generator until the next program scan. During the next scan Inverter B0004 will sense the ON state from the Start/Stop latch and remove the reset signal applied to the PWM generator B0006. The PWM generator then 'see's' the reset signal removed and a high level on its Trigger input, allowing it to start generating pulses.

When the Activation signal is removed the Deceleration Timer B0002 begins it's time out function and when the elapsed time reaches the TON (DW2) value it will set it's output active. This in turn resets the Start/Stop latch which disables the Trigger input to the PWM controller and sets the Reset signal, stopping the pulse generation.

The output from the PWM controller has been directed to physical output Q02, one of the high speed outputs.

NOTE: The APBSoftware forces the use of either Q02 or Q03 when using the PTO, PWM or ACC function blocks. It does not verify that these blocks are used on DC powered, solid state outputs.

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Summary

The APB controller uses functional blocks to implement control sequences and in high speed applications it may be necessary to understand the overall processing performed by the controller. In particular, the overall processing times and sequence of processing may become critical in certain high speed applications.

Digital filtering is used for both analog and digital input signals which will eliminated switch contact noise and smooth analog input signals. The sampling time may be set between 20 msec to 1 second using the APBSoftware design tools. In all applications the digital filtering used on inputs must be considered if input signals are greater than ~ 50 hertz.

The APB controller provides 4 high speed digital inputs and 2 high speed digital outputs which are not subject to the restrictions caused by the overall program processing times. The inputs are specifically used to drive counter functions but these may be used to implement simple pulse capture functions to allow high speed signals to be processed by other function blocks.

The high speed outputs are specific to pulse generation and functions are available to generate either a fixed number or a continuous stream of pulses with a variable duty cycle. The ACC function block expands the pulse generation to perform acceleration and deceleration useful in motor control.

To illustrate some of the techniques discussed an application was shown that addresses a ramp up and ramp down of a PWM signal duty cycle.

References

http://en.wikipedia.org/wiki/Aliasing

AP-2 Position and Speed

Ingram Products Inc.,
8725 Youngerman Court
Suite 206
Jacksonville, FL 32244
888-875-2221
West Coast Sales: 951-200-3592
e-mail: sales@ingramproducts.com

Web Site: www.ingramproducts.com